What is claimed is:

1. A processor, comprising:

a physical register file populated by a number of registers;

an instruction decoder;

a register alias table coupled to the instruction decoder;

an active list populated by a number of entries, the entries include an old field and a new field; and

a free list of unallocated physical registers reclaimed from said active list.

2. The processor of claim 1, further comprising an instruction window buffer having dispatched instructions.

3. The processor of claim 2, wherein said dispatched instructions correlate to evicted allocated physical registers, said free list reclaims said evicted physical registers when said dispatched instructions retire.

4. The processor of claim 1, wherein said instruction writes to said allocated physical register.

5. The processor of claim 1, wherein said allocated physical register is allocated from said free list.

6. The processor of claim 1, further comprising a misprediction condition wherein said free list reclaims mispredicted said allocated physical registers from said new field.

7. The processor of claims 1, further comprising a bit field within said active list, said bit field comprising at least one bit to indicate whether the instruction is retired correctly.

8. A method for recovering registers in a processor, comprising:

detecting an exception correlating to an instruction associated with an entry on an active list;

moving a pointer on said active list to an old field and a new field after said entry; and

reclaiming allocated physical registers in said new field to a free list.

9. The method of claim 8, further comprising flushing instructions in an instruction window buffer after said instruction associated with said misprediction condition.

10. The method of claim 9, further comprising overwriting entries in said active list.

11. The method of claim 8, further comprising allocating unallocated physical registers from said free list to a register alias table.

12. The method of claim 11, further comprising moving evicted physical registers from said register alias table to said active list.

13. A method for recovering registers in a processor, comprising:
reading a bit in an active list; and
reclaiming a physical register from said active list to a free list according to said bit.

14. The method of claim 13, further comprising overwriting an entry in said active list.

15. The method of claim 13, further comprising setting said bit during a misprediction condition.

16. The method of claim 13, wherein said reclaiming includes reading said physical register from an old field in said active list.

17. The method of claim 13, wherein said reclaiming includes reading said physical register from a new field in said active list.

18. The method of claim 13, wherein said reading includes reading said bit in a bit field within said active list.

19. A register renaming apparatus within a processor, comprising:
a register alias table;
a first set of registers renamed by said register alias table;

an active list having an old field and a new field that correlate to said registers; and
a free list comprising a second set of registers reclaimed from said active list.

20. The apparatus of claim 19, wherein said said first set of registers correlate to non-retired instructions.

21. The apparatus of claim 19, wherein said active list includes a bit field.

22. The apparatus of claim 19, further comprising a pointer for said active list.